What is claimed is:

1. A method of switching between a first clock and a second clock, said second clock having a slower rate than that of said first clock, said method comprising the steps of:

receiving a first switch command signal to switch from said first clock to said second clock;

generating a first mask signal so as to mask said first clock until a next positive transition of said second clock;

measuring a first time duration said first mask signal was active to determine the ambiguity of a first cycle of said second clock;

outputting said second clock as an output clock;

receiving a second switch command signal to switch from said second clock to said first clock;

generating a second mask signal having a second time duration of one second clock period less said first time duration to mask said second clock so as to compensate for said ambiguity of said first cycle of said second clock; and

outputting said first clock as said output clock.

2. The method according to claim 1, wherein said output clock is utilized as a Bluetooth clock signal.

3. The method according to claim 1, wherein said second command signal is received one cycle of said second clock before a desired clock switch time.

4. The method according to claim 1, wherein said first mask signal functions to generate glitch free switching between said first clock and said second clock and to indicate the ambiguity of said first cycle of said second clock.

5. A method of switching between a fast clock and a slow clock, said fast clock having a higher clock rate than that of said slow clock, said method comprising the steps of:

providing a counter loaded initially with a value corresponding to a period of said slow clock;

receiving a first command to switch from said fast clock to said slow clock;

in response to said first command, generating a first mask signal until a first low to high transition of said slow clock for masking said fast clock;

enabling count down of said counter while said mask signal is active and freezing said counter thereafter;

switching from said fast clock to said slow clock;

receiving a second command to switch from said slow clock to said fast clock;

in response to said second command, enabling the countdown of said counter to zero;

generating a second mask signal until said counter reaches zero; and

switching from said slow clock to said fast clock.

6. The method according to claim 5, wherein said output clock is utilized as a Bluetooth clock signal.

7. The method according to claim 5, wherein said second command signal is received one cycle of said second clock before a desired clock switch time.

8. The method according to claim 5, wherein said first mask signal functions to generate glitch free switching between said fast clock and said slow clock and to indicate the ambiguity of said first cycle of said slow clock.

9. A method of switching between a fast clock and a slow clock, said fast clock having a higher clock rate than that of said slow clock, said method comprising the steps of:

receiving a first command to switch from said fast clock to said slow clock;

switching from said fast clock to said slow clock;

measuring the ambiguity of a first slow clock cycle;

receiving a second command to switch from said slow clock to said fast clock;

compensating the last cycle of said slow clock by an amount corresponding to said previously measured ambiguity; and

switching from said slow clock to said fast clock.

10. The method according to claim 9, wherein said output clock is utilized as a Bluetooth clock signal.

11. The method according to claim 9, wherein said second command signal is received one cycle of said second clock before a desired clock switch time.

12. A clock switching apparatus, comprising:

a multiplexer for switching between a slow clock and a fast clock input thereto;

a gate for gating the output of said multiplexer with a mask signal, said gate adapted to produce an output clock signal;

a counter adapted to count down a period of said slow clock;

a timing and control circuit adapted to:

receive a first command to switch from said fast clock to said slow clock;

in response to said first command, first activate said mask signal until a first low to high transition of said slow clock;

enable countdown of said counter while said mask signal is active and freezing said counter thereafter;

configure said multiplexer to output said slow clock;

receive a second command to switch from said slow clock to said fast clock;

in response to said second command, enable the countdown of said counter to zero;

second activate said mask signal until said counter reaches zero; and

configure said multiplexer to output said fast clock.

13. The apparatus according to claim 12, wherein said output clock signal is utilized as a Bluetooth clock signal.

14. The apparatus according to claim 12, wherein said timing and control circuit is implemented as a state machine.

15. The apparatus according to claim 12, wherein said counter is loaded with a value corresponding to the period of said slow clock before said first activation of said mask signal.

16. The apparatus according to claim 12, wherein said second command is received one cycle of said slow clock before a desired clock switch time.

17. The apparatus according to claim 12, wherein said mask signal functions both to generate glitch free switching between said fast clock and said slow clock and to indicate the ambiguity of said first cycle of said slow clock.

18. The apparatus according to claim 12, wherein said gate comprises an OR gate.